UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,687	03/15/2004	Yao-Chia Yeh	4425-350	8647

7590 07/13/2005

LOWE HAUPTMAN GILMAN & BERNER, LLP
Suite 310
1700 Diagonal Road
Alexandria, VA 22314

EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	10/799,687	YEH ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed March 15, 2004.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a second oxide layer above a dummy wafer", as recited in claim 1, and "a third oxide layer above a dummy wafer", as recited in claim 11, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose sentences in the specification are: "The photolithography is the most influenced step of the semiconductor processes, which determines the structure about MOS transistor." (pg. 2); "In which, utilizing a reactive gas that has a fluorine atom such as CF_4." (pg. 9); "As a result, the oxidation is performed on the surface of the silicon chip so that the silicon atom on the silicon chip is on the reactant." (pg. 10); "That is, utilizing the method of the present invention has overcame the problem with the resolution of the word line of the gate is limited to the width of the photoresist layer, and shrinking the dimension of the gate to reach an advanced process by the economical and convenient method." NOTE: There are many other confusing language/grammatical errors throughout the specification other than those stated above that need to be corrected. A specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required.

Claim Objections

Claims 5, 6, 12 and 13 are objected to because of the following informalities:

Claim 5 recites the limitation of "said first oxide layer comprises utilizing a method of thermal oxidation to deposit." Similarly, claim 12 recites the limitation of "said second oxide layer comprises utilizing a method of thermal oxidation to deposit." These limitations need to be rewritten in idiomatic English.

Claims 6 and 13 recite the limitation of "utilizing a method of conformal to deposit." This limitation needs to be rewritten in idiomatic English.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation of "wherein said thickness of said first oxide layer is in accordance with the thickness of a second oxide layer above a dummy wafer". Similarly, claim 11 recites the limitation of "wherein said thickness of said second oxide layer is in accordance with the thickness of a third oxide layer above a dummy wafer". It is not understood what is meant by forming the one oxide layer "in accordance" with a thickness of another oxide layer.

Claim 3 recites the limitation of "said semiconductor gate comprises a polysilicon layer and a gate oxide layer thereon." However, it is unclear as to which oxide layer "gate oxide layer" intends to refer because Applicant's specification and drawings disclose gate oxide layer 205 as being *under* the polysilicon layer 207, not *on* it and the only oxide layer disclosed by the Applicant to be on the polysilicon layer is already recited in claim as "a first oxide layer."

Claim 4 recites the limitation of "wherein comprises a plurality of ions doped therein." *What* comprises a plurality of ions doped therein? And what/where is "therein"? This claim is completely unintelligible.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheah et al. (US 6,475,842) in view of Wang et al. (US 20030109071).

Regarding claim 1, Cheah discloses providing a semiconductor structure (110), forming a semiconductor gate (410) on the semiconductor structure, forming a first oxide layer (510) on a surface of the semiconductor gate and semiconductor structure, and removing the first oxide layer with an etching solution (Fig. 4-6; col. 3, ln. 39 – col. 4, ln. 65). Cheah does not disclose forming the thickness of the first oxide layer in accordance with a thickness of a second oxide layer above a dummy wafer. Like Cheah, Wang discloses forming an oxide layer on a semiconductor substrate. Wang teaches that it is beneficial to use dummy (monitor) wafers during the oxide layer deposition process, wherein the dummy wafers serve the purpose of being able to monitor the film formation process, which allows the oxide films on the device wafers to be formed having a specified thickness. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the dummy/monitor wafer process of Wang during formation of the oxide layer of Cheah because Wang teaches that by using these monitor wafers, oxide layers of a specified thickness can be reliably grown on the device wafers.

Regarding claim 2, Cheah discloses a semiconductor substrate having plurality of isolation zones (215) in therein (col. 3, ln. 43-45).

Regarding claim 3, Cheah discloses that the semiconductor gate includes a polysilicon layer (410) and a gate oxide layer (220).

Regarding claim 4, Cheah discloses that the substrate has a plurality of ions (640) doped therein.

Regarding claim 5, Cheah discloses that the first oxide layer is formed by thermal oxidation (col. 4, ln. 31-50).

Regarding claim 6, Cheah discloses that the first oxide layer is formed conformally (Fig. 5).

Regarding claims 7 and 8, Cheah discloses that the etching solution is a DHF solution (HF in deionized water) (col. 4, ln. 56-60).

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheah et al. (US 6,475,842) in view of Wang et al. (US 20030109071) as applied to claim 1 above, and further in view of Wu (US 5,985,737).

Regarding claims 9 and 10, Cheah discloses using a hydrofluoric etching solution, but Cheah does not disclose using a buffered oxide etch. Like Cheah, Wu discloses using an etching solution to remove silicon oxide on a semiconductor substrate. Wu teaches that it is beneficial to use a buffered oxide etch of a HF/NH_4F solution because diluted hydrofluoric (HF) solution is used because it has the advantage of dissolving silicon dioxide without attacking silicon and the ammonium fluoride (NH.sub.4 F) is added to the HF solution in order to slow down the etch rate into a more controllable process (col. 3, ln. 47-53). At the time of the invention, it would have

been obvious to one of ordinary skill in the art to use a HF/NH_4F buffered oxide solution to etch the oxide layer of Cheah because Cheah discloses using a HF solution and Wu teaches that it is advantageous to use a HF/NH_4F buffered oxide etch because it can dissolve the silicon dioxide without attacking silicon in a slower, more controllable process.

Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6,136,657) in view of Wang et al. (US 20030109071) and the admitted prior art.

Regarding claim 11, Yang discloses providing a semiconductor substrate (1), forming a first oxide layer (10) on the substrate, forming a polysilicon layer (13a) on the first oxide layer, etching a portion of the polysilicon layer and the first oxide layer until a portion of the substrate is exposed, performing an oxidation on a surface of the polysilicon layer, the first oxide layer and the substrate to form a second oxide layer (18) on the surface of the polysilicon layer, first oxide layer and the substrate, and removing the second oxide layer with an etching solution (Fig. 5a-6c; col. 5, ln. 21 – col. 6, ln. 21). Yang does not disclose forming the thickness of the first oxide layer in accordance with a thickness of a second oxide layer above a dummy wafer. Like Yang, Wang discloses forming an oxide layer on a semiconductor substrate. Wang teaches that it is beneficial to use dummy (monitor) wafers during the oxide layer deposition process, wherein the dummy wafers serve the purpose of being able to monitor the film formation process, which allows the oxide films on the device wafers to be formed having a specified thickness. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the dummy/monitor wafer process of Wang during formation of the oxide layer of Yang because Wang teaches that by using these monitor wafers, oxide layers of a specified thickness can be reliably grown on the device wafers. Further regarding claim 11, Yang discloses that the

polysilicon layer and first oxide layer are patterned by "photoetching" but does not specifically describe the steps involved in this process. As is disclosed by the admitted prior art (specification page 3-4), it is well-known and conventional in the art to pattern gate and gate oxide layers by forming a photoresist on the gate (polysilicon) layer, patterning the photoresist layer, etching the gate and gate oxide layers using the patterned photoresist layer as a mask, and removing the photoresist layer. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the photolithography method disclosed in the admitted prior art to pattern the gate and gate oxide of Yang because Yang discloses using "photoetching" and because the photolithography process is well-known and conventional in the art.

Regarding claim 12, Yang discloses that the first oxide layer is formed by thermal oxidation (col. 5, ln. 66 – col. 6, ln. 10).

Regarding claim 13, Yang discloses that the first oxide layer is formed conformally (Fig. 6C).

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6,136,657) in view of Wang et al. (US 20030109071) and the admitted prior art as applied to claim 11 above, and further in view of Cheah et al. (US 6,475,842).

Regarding claims 14 and 15, Yang discloses using a wet etching solution to remove the second oxide layer, but does not disclose any particular etching solution. Like Yang, Cheah discloses removing a silicon oxide layer using wet etching. Cheah teaches that this layer can be successfully removed by using a DHF (HF in deionized water) solution. At the time of the invention, it would have been obvious to one of ordinary skill in the art to remove the second

oxide layer of Yang using the DHF solution taught by Cheah because Yang discloses using wet etching and Cheah teaches that the DHF solution can successfully etch silicon oxide.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6,136,657) in view of Wang et al. (US 20030109071) and the admitted prior art as applied to claim 11 above, and further in view of Wu (US 5,985,737).

Regarding claims 16 and 17, Yang discloses using a wet etching process to remove the second oxide layer, but Yang does not disclose using a buffered oxide etch. Like Yang, Wu discloses using an etching solution to remove silicon oxide on a semiconductor substrate. Wu teaches that it is beneficial to use a buffered oxide etch of a HF/NH_4F solution because diluted hydrofluoric (HF) solution is used because it has the advantage of dissolving silicon dioxide without attacking silicon and the ammonium fluoride (NH.sub.4 F) is added to the HF solution in order to slow down the etch rate into a more controllable process (col. 3, ln. 47-53). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a HF/NH_4F buffered oxide solution to etch the oxide layer of Yang because Yang discloses using a wet etching solution and Wu teaches that it is advantageous to use a HF/NH_4F buffered oxide etch because it can dissolve the silicon dioxide without attacking silicon in a slower, more controllable process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 (571-273-8300 as of July 15, 2005).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
July 8, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800